

**REMARKS**

Claims 1-29 are all the claims presently pending in the application. Claims 1-11 have been amended to more clearly define the invention and claims 24-29 have been added. Claims 12-23 have been withdrawn from prosecution. Of the remaining claims, claims 1, 6 and 24 are independent.

These amendments are made only to more particularly point out the invention for the Examiner and not for narrowing the scope of the claims or for any reason related to a statutory requirement for patentability.

Applicants also note that, notwithstanding any claim amendments herein or later during prosecution, Applicants' intent is to encompass equivalents of all claim elements.

Claim 9 stands rejected under 35 U.S.C. § 112, second paragraph as indefinite. Claims 1-2 stand rejected under 35 U.S.C. § 102(e) as being anticipated by Park et al. (U.S. Patent No. 6,380,559). Claims 3-5 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Park. Claims 6-11 stand rejected under 35 U.S.C. § 103(a) as being unpatentable in view of Park in view of Kim et al. (U.S. Patent No. 5,917,564).

Briefly, Park et al. can be overcome by filing a verified English translation of the priority document, as Park et al. has an effective date of June 2, 2000 (e.g., its U.S. filing date) whereas the present application has an effective date (e.g., its priority date) of October 26, 1999.

While Applicants may file a verified translation of the priority document which will remove the Park et al. as a reference, Applicants respectfully submit that the Park et al. reference and the Kim et al. reference are clearly deficient on the merits. Thus, these rejections are respectfully traversed in the following discussion.

## **I. THE CLAIMED INVENTION**

The claimed invention is directed to an active matrix liquid crystal display panel including a gate electrode on a substrate, a pixel electrode on the substrate, a channel layer over the gate electrode, and a passivation layer on the channel layer and covering the top and sides of the channel layer.

Conventional active matrix liquid crystal display panels require protection for the channel layer from the liquid crystal material. These display panels provide a passivation layer on source, drain and pixel electrodes to protect the side of the channel layer. However, these active matrix liquid crystal display panels require at least five lithographic steps (page 6, lines 11-25).

By contrast, the active matrix liquid crystal display panel of the present invention provides protection of the top and sides of the channel layer while reducing the number of lithographic steps required to produce the panel. In particular, the active matrix liquid crystal display panel of the present invention forms the passivation layer on the channel layer and protects the top surface and sides of the channel layer.

As explained by the specification, these features are important for protecting the channel layer from the liquid crystal while reducing the number of lithographic steps required to produce the panel.

## **II. THE 35 U.S.C § 112, SECOND PARAGRAPH REJECTION**

The Examiner alleges that claim 9 is indefinite. This Amendment amends claim 9 to depend from claim 8. Applicants respectfully request withdrawal of this rejection.

### III. THE PRIOR ART REJECTIONS

#### A. The 102(e) Park et al. reference rejection

Regarding the rejection of claims 1-2, the Examiner alleges that the Park et al. reference teaches the claimed invention. Applicants submit, however, that there are elements of the claimed invention which are neither taught nor suggested by this reference.

The Park et al. reference does not teach or suggest the features of the present invention including: 1) a passivation layer covering the side surfaces and a top surface of the amorphous silicon layer; 2) the source and drain electrodes contacting the amorphous silicon layer through openings in the passivation layer; and 3) the source electrode contacting the pixel electrode. As explained above, these features are important for protecting the channel layer from the liquid crystal while reducing the number of lithographic steps required to produce the panel.

The Park et al. reference discloses a thin film transistor array substrate for a liquid crystal display. More specifically, in the same manner as described by the specification at page 6, lines 11 - 25 and shown in Prior Art Fig. 2D, the Park et al. reference (e.g., see Fig. 4 thereof) discloses forming the passivation layer 70 over the source 65 and drain 66 electrodes and leaving the edge of the channel layer 42 exposed (see above gate line 22 in Fig. 4 of Park et al.). Therefore, the Park et al. reference leaves the channel layer exposed to the liquid crystal material and is subject to a problem solved by the present invention and described in the specification at, for example, page 7, lines 4-10.

Additionally, contrary to the Examiner's allegation, the Park et al. reference does not teach or suggest the source and drain electrodes contacting the amorphous silicon layer through openings in the passivation layer. Rather, the Park et al. reference discloses the

source electrode 65 and the drain electrode 66 formed on and, therefore, directly contacting the amorphous silicon layer 42.

Indeed, the passivation layer 70 is not even positioned between the source and drain electrodes in the panel disclosed by the Park et al. reference. Therefore, there is no need to form openings in the passivation layer 70 to enable the source and drain electrodes to contact the amorphous silicon layer because the source and drain electrodes 65 and 66 of the Park et al. reference are formed directly on the amorphous silicon layer 42.

Lastly, contrary to the Examiner's allegation, the Park et al. reference does not teach or suggest a source electrode in contact with the pixel electrode. Rather, the Park et al. reference discloses a drain electrode 66 in contact with the pixel electrode 82.

Therefore, contrary to the allegations of the Examiner, the Park et al. reference does not teach or suggest each and every element of the claimed invention. Therefore, the Examiner is respectfully requested to withdraw this rejection of claims 1-2.

#### **B. The 103(a) Park et al. reference rejection**

Regarding the rejection of claims 3-5, the Examiner alleges that it would have been obvious to modify the Park et al. reference to form the claimed invention. Applicants submit, however, that it would not have been obvious to modify the Park et al. reference and even if modified, the modification would not teach or suggest each and every element of the claimed invention.

Applicants submit that this reference would not have been modified as alleged by the Examiner. Indeed, the Examiner does not even suggest a modification to arrive at the claimed invention. The Examiner merely alleges that Fig. 4 of the Park et al. reference

discloses the shape of the a-Si layer that is substantially the same as the gate insulating film. However, the perspective of the view of Fig. 4 is parallel to the surface of the substrate.

In stark contrast, the present invention recites that the shapes are substantially the same when viewed perpendicular to the surface of the substrate. For example, Figs. 3A - 3D show a perspective view which is perpendicular to the substrate. In particular, Fig. 3B in combination with Figs. 4B - 4D, illustrate that a gate insulating film 34 and an a-Si layer 35 which are substantially the same shape.

Fig. 4 of the Park et al. reference only illustrates a cross-section of the layers making up the device disclosed by the Park et al. reference, but does not illustrate the shape of the a-Si layer 42 or the gate insulating film 39 at all.

Further, contrary to the Examiner's allegation, Fig. 4 of the Park et al. reference shows that the a-Si layer 42 has a discontinuity at the pixel electrode 82 where the pixel electrode 82 contacts the gate insulating film 30. Therefore, even if the device illustrated in Fig. 4, was provided with a perspective view which is parallel with the substrate (rather than the current cross-section view) clearly the shape of the a-Si layer 42 is not substantially the same shape as the gate insulating film 30.

Further, regarding claim 5, the Park et al. reference does not teach or suggest doping the a-Si layer 42 in the regions that contact the source electrode 65 and the drain electrode 66. Indeed, the Examiner makes absolutely no attempt to cite any portion of the Park et al. reference to allege that the Park et al. reference makes such a disclosure. Clearly, the Examiner has failed to make a prima facie case of obviousness.

Therefore, the Examiner is respectfully requested to withdraw this rejection of claims 3-5.

**C. The Park et al. reference in view of the Kim et al. reference**

Regarding the rejection of claims 6-11, the Examiner alleges that the Kim et al. reference would have been combined with the Park et al. reference to form the claimed invention. Applicants submit, however, that these references would not have been combined and even if combined, the combination would not teach or suggest each and every element of the claimed invention.

Applicants submit that these references would not have been combined as alleged by the Examiner. Indeed, the references are directed to completely different matters and problems.

Specifically, the Park et al. reference is directed to ensuring suitable contacts between the electrode components and providing a suitable opening ratio (col. 1, lines 48 - 53).

In contrast, the Kim et al. reference is specifically directed to reducing the susceptibility to image-sticking (col. 3, lines 31-35). Therefore, since the Kim et al. reference is directed to the completely different problem of reducing susceptibility to image-sticking and is not at all concerned with ensuring suitable contacts between the electrode components and providing a suitable opening ratio as disclosed by the Park et al. reference, one of ordinary skill in the art would not have been motivated to modify the teachings of the Park et al. reference based upon the disclosure of the Kim et al. reference. Thus, the references would not have been combined, absent hindsight.

Further, Applicants submit that the Examiner can point to no motivation or suggestion in the references to urge the combination as alleged by the Examiner. Indeed, the Examiner does not even support the combination by identifying a reason for combining the references.

Moreover, the Kim et al. reference, like the Park et al. reference, does not teach or

suggest the features of the present invention including: 1) a passivation layer covering the side surfaces of the amorphous silicon layer; 2) the source and drain electrodes contacting the amorphous silicon layer through openings in the passivation layer; and 3) the source electrode contacting the pixel electrode. As explained above, these features are important for protecting the channel layer from the liquid crystal while reducing the number of lithographic steps required to produce the panel.

Clearly, these novel features are not taught or suggested by the Kim et al. reference. Indeed, the Kim et al. reference is completely unrelated to the claimed invention.

Rather, the Kim et al. reference discloses a channel layer (a-Si layer) 16 which is exposed on the sides. As a result, the channel layer 16 is subject to the same problems experienced by the Park et al. reference and which are solved by the present invention by providing a passivation layer which covers the side surfaces of the amorphous silicon layer.

Further, the Kim et al. reference also does not disclose the source and drain electrodes contacting the amorphous silicon layer 16 at all, let alone contacting the layer through openings in a passivation layer.

Lastly, as shown in Fig. 9b, the Kim et al. reference discloses that the drain contacts the pixel electrode, as opposed to the source electrode as recited by the present claims.

Therefore, the Examiner is respectfully requested to withdraw this rejection of claims 6-11.

#### **IV. FORMAL MATTERS AND CONCLUSION**

In view of the foregoing amendments and remarks, Applicants respectfully submit that claims 1-29, all the claims presently pending in the Application, are patentably distinct

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over the prior art of record and are in condition for allowance. The Examiner is respectfully requested to pass the above application to issue at the earliest possible time.

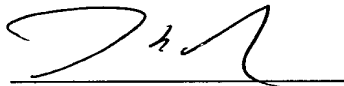
Should the Examiner find the Application to be other than in condition for allowance, the Examiner is requested to contact the undersigned at the local telephone number listed below to discuss any other changes deemed necessary in a telephonic or personal interview.

The Commissioner is hereby authorized to charge any deficiency in fees or to credit any overpayment in fees to Attorney's Deposit Account No. 50-0481.

Respectfully Submitted,

Date:

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